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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,536	10/23/2003	Yasushi Hayakawa	244342US2	9083

22850 7590 10/13/2005

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EXAMINER	
CUNNINGHAM, TERRY D	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,536	HAYAKAWA, YASUSHI	
	Examiner	Art Unit	
	Terry D. Cunningham	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 22 August 2005 has been entered.

Specification

The amendment filed 16 March 2005 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is the language of claim 1 reciting that the "voltage signal" is "from the exterior of said bias voltage generating circuit". There is nothing disclosed in the original specification establishing that this signal is in any "from the exterior".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification fails to provide adequate written description for the new language of claim 1 reciting that the "voltage signal" is "from the exterior of said bias voltage generating circuit", for similar reasons as discussed above.

Examiner has fully considered Applicant's remarks for the above New Matter objection and rejection and has not found them to be persuasive. . Applicant is arguing the merits of Enablement, not Written Description. The rejection is made under the Written Description requirement of 35 U.S.C. § 112. The mere fact that one skilled in the art may know how to make and use an external "voltage signal", does not necessitate that one skilled in the art would be able to divine that this is what the broad disclosure is intended to disclose, despite such a broad description. Clearly, the disclosure shown in the figure and discussed in the specification for the "voltage signal" is broad enough to allow for both an internal or external supply thereof. Thus, the new specific recitation is deemed New Matter.

Claims 1-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The claims now recite that the "first bias voltage varies in accordance with changes in an absolute value of said voltage signal" Vref. While the operation is discussed in the specification, it is not seen that the circuit can operate as disclosed. As seen in the circuit of Fig. 2, for example, transistor M2 constitutes a current source output. Further, transistor M3 is seen to operate as a variable resistance responsive to Vref. Transistor M4 is connected as a diode. Since

only current is provided to diode-connected transistor M4 and not a clamping voltage, transistor M4 will float at the threshold level thereof. Thus, it is not seen that the voltage biasn can vary "in accordance" with Vref. Therefore, it is not seen that the specification adequately enables one skilled in the art to make and use the invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In line 3, it is not understood how a circuit can be "standing" between other elements. Thus, it is not seen that the claim provides any connections for the "third transistor".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 8 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Takehara (USPN 4,480,231).

With respect to claims 1 and 2, Takehara discloses a circuit comprising: "a first current generating part (36-40)" having "a current source (38)" and "a current mirror (36 and 40)"; "a first transistor (48) of a first conductivity type"; "a first potential (Vss)"; "a second transistor (34) of a second conductivity type different from said first conductivity type"; "a second potential (Vdd) different from said first potential"; "a voltage signal (at gate of 46, generated by 42 and 44)"; and "a first bias (at drain of 34)", all connected and operating as recited by Applicant.

With respect to claims 1, 3 and 4, Takehara discloses a circuit comprising: "a first current generating part (24 and 34-40)" having "a current source (28)", "a first current mirror (36 and 40)" and "a second current mirror (24 and 34)"; "a first transistor (22) of a first conductivity type"; "a first potential (Vdd)"; "a second transistor (28) of a second conductivity type different from said first conductivity type"; "a second potential (Vss) different from said first potential"; "a voltage signal (at gate of 22, generated by 30 and 32)"; "a first bias voltage (at drain of)"; "a third transistor (46)"; "other voltage signal (at gate of 46, generated by 42 and 44)", all connected and operating as recited by Applicant.

With respect to claims 1 and 5, Takehara discloses a circuit comprising: "a first current generating part (36-40)"; "a first transistor (48) of a first conductivity type"; "a first potential (Vss)"; "a second transistor (34) of a second conductivity type different from said first conductivity type"; "a second potential (Vdd) different from said first potential"; "a voltage signal (INPUT) is inputted (via 42) to said control electrode of said first transistor from the exterior of said bias voltage generating circuit"; "a first bias (at drain of 34)", "a second current

generating part (24)"; "a fourth transistor (22) of said second conductivity type"; "a fifth transistor (28) of said first conductivity type" wherein "said voltage signal (INPUT) is inputted (via 20 and 32) to said control electrode of said fourth transistor (22) and a potential at said second current electrode of said fifth transistor functions as a second bias voltage", all connected and operating as recited by Applicant.

With respect to claims 1 and 8, Takehara discloses a circuit comprising: "a first current generating part (36-40)"; "a first transistor (48) of a first conductivity type"; "a first potential (Vss)"; "a second transistor (34) of a second conductivity type different from said first conductivity type"; "a second potential (Vdd) different from said first potential"; "a voltage signal (INPUT) is inputted (via 42) to said control electrode of said first transistor from the exterior of said bias voltage generating circuit"; "a first bias (at drain of 34)", "seventh transistor (24)"; "a eighth transistor (22) of said second conductivity type"; "a ninth transistor (28) of said first conductivity type" wherein "said voltage signal (INPUT) is inputted (via 20 and 32) to said control electrode of said fourth transistor (22) and a potential at said second current electrode of said fifth transistor functions as a second bias voltage", all connected and operating as recited by Applicant.

With respect to claims 1 and 9, Takehara discloses a circuit comprising: "a first current generating part (36-40)"; "a first transistor (48) of a first conductivity type"; "a first potential (Vss)"; "a second transistor (34) of a second conductivity type different from said first conductivity type"; "a second potential (Vdd) different from said first potential"; "a voltage signal (at gate of 46, generated by 42 and 44)"; "a first bias (at drain of 34)"; "a differential amplifier circuit (20-36) having a tenth transistor (24) including a first and second current electrodes and a control electrode as a current circuit, wherein a reference voltage signal

(INPUT) and an input voltage signal (OUTPUT) are inputted to said differential amplifier circuit, said reference voltage signal (INPUT) is also inputted (via 42) to said control electrode of said first transistor as said voltage signal and said first bias voltage (at gate and drain of 34) is inputted to said control electrode of said tenth transistor", all connected and operating as recited by Applicant.

Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Narendra et al. (USPN 6,518,833).

With respect to claim 1, Narendra et al. disclose, in Fig. 1, a circuit comprising: "a first current generating part (lower transistor of branch 106)"; "a first transistor (middle transistor of branch 106) of a first conductivity type"; "a first potential (ground)"; "a second transistor (118) of a second conductivity type different"; "a second potential (Vcc) different from said first potential"; "a voltage signal (at gate of middle transistor of branch 106)"; and "a first bias (Vcc - Va)", all connected and operating as recited by Applicant..

Examiner has fully considered Applicant's remarks for the above rejection and has not found them to be persuasive. As seen, since the circuitry (i.e., branch 20 108 and R1) generating the voltage at the gate of the middle transistor of branch 106 is not included as part of the "bias voltage generating circuit", such is from the "exterior". Also, since diode 118 is clamped to the middle transistor of branch 106, due to R2, the "first bias voltage" will change with "the voltage signal".

With respect to claims 2-4, insofar as the claims can be understood, Narendra further discloses, "a current source (lower transistor of branch 104)"; "a first current mirror (lower transistors of branches 102 and 106)"; "a second current mirror (108 and 110)"; and "a third transistor (middle transistor of branch 102)".

With respect to claims 1, 4 and 8, since the "bias voltage generating circuit" is being read as only including the circuitry in branches 104 and 106 Narendra et al., the voltage generated by the middle transistor of branch 102 would be "from the exterior of said bias voltage generating circuit".

With respect to claims 2 and 3, the reference to Narendra et al. is seen to meet the claim language insofar as understood based on the original specification.

Allowable Subject Matter

Claims 7, 8, 10 and 11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st and 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

With respect to claims 7, 8 and 11, none of the cite prior art references disclose the circuit recited in claims 1, 5 and 6 and further disclose that the "first current generating part" has a "current source" and "a first current mirror" and that the "second current generating part" further has "a second current mirror" and "a third current mirror".

With respect to claim 10, since element 22, 24 and 28 of Takehara are being used to read on other recited elements, it is not seen that such further discloses "a differential amplifier". It would not be seen to be proper to read 22, 24 and 28 as being part of two differently claimed elements.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terry Cunningham whose telephone number is 571-272-1742. The examiner can normally be reached on Monday-Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Terry D. Cunningham
Primary Examiner
Art Unit 2816

TC
October 4, 2005